What is claimed is:

1. A method of fabricating a stacked-gate nonvolatile semiconductor memory device having a floating gate and a control gate, including the steps of:

forming a tunnel insulating layer in a device forming region defined in a semiconductor substrate;

forming an impurity-doped silicon layer in said tunnel insulating layer;

forming a protective layer at a surface of said silicon layer;

laminating a lower layer and an upper layer of a laminated mask layer on said protective layer in order;

forming said upper layer into a desired pattern;

forming a second upper layer on said pattern of said upper layer;

etching said second upper layer and leaving said second upper layer only on a side surface of said first upper layer;

etching said lower layer using said first and second upper layers as masks;

forming a silicon pattern by etching said silicon layer using said lower layer as a mask;

forming a second protective layer 121 covering a surface of said silicon pattern exposed; and

etching out said lower layer.

2. The fabrication method according to claim 1, further including the steps of:

removing said protective layer present at the surface

of said silicon pattern after the step of etching out said lower layer;

forming a capacitance insulating layer at the surface of said silicon pattern;

forming a conductive layer on said capacitance insulating layer; and

forming a control gate with said conductive layer and forming a floating gate with said silicon pattern by etching said conductive layer, said capacitance insulating layer and said silicon pattern in order into a desired pattern.

3. The fabrication method according to claim 1, wherein said silicon layer is a polysilicon layer or a metal polyside layer.

4. The fabrication method according to claim 2, wherein said silicon layer is a polysilicon layer or a metal polyside layer.

5. The fabrication method according to claim 3, wherein said lower layer is a silicon nitride layer and said first and second upper layers are silicon oxide layers.

6. The fabrication method according to claim 4, wherein said lower layer is a silicon nitride layer and said first and second upper layers are silicon oxide layers.

7. The fabrication method according to claim 1, wherein said protective layer is a thermal oxidation silicon oxide layer obtained by subjecting the surface of said polysilicon layer to a heat treatment.

8. The fabrication method according to claim 1, wherein said silicon nitride layer is etched out by a

phosphoric acid solution.

9. The fabrication method according to claim 8, wherein a thickness of said silicon nitride layer is set greater than a sum of a thickness of said silicon nitride layer to be etched and a thickness of said silicon nitride layer to be etched at a time of etching said polysilicon layer.

10. The fabrication method according to claim 9, wherein a thickness of said first upper layer is set greater than a thickness of said second upper layer.

11. The fabrication method according to claim 10, wherein said thickness of said first upper layer is equal to or greater than twice said thickness of said second upper layer.